

CLAIMS

I claim:

1. A programmable logic array (PLA) comprising:

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a plurality of sub-program logic arrays (sub-PLAs) comprising at least a diode wherein at least one of said sub-PLAs includes a share-midterm-input (SMI) logic-bypass circuit for calculating a common logic truth value to conditionally provide a predefined sub-PLA vector without activating said sub-PLA.

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2. A programmable logic array (PLA) comprising:

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a plurality of sub-program logic arrays (sub-PLAs) comprising at least a diode wherein at least one of said sub-PLAs includes an input comparator for comparing a set of new inputs to said sub-PLA with a set of most recent inputs for said sub-PLA and to activate said sub-PLA only when said set of new inputs are different from said set of most recent inputs.

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3. A programmable logic array (PLA) comprising:

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a plurality of sub-program logic arrays (sub-PLAs) comprising at least a diode wherein each of said sub-PLAs includes an array of logic-operation circuits and a plurality of input and output lines;

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everyone of said input lines connected to a unique set of said logic-operation circuits whereby each of said input lines connected to a different set of logic-operation circuits from every other input lines.

4. A programmable logic array (PLA) comprising:

a plurality of sub-program logic arrays (sub-PLAs) comprising at least a diode wherein each of said sub-PLAs includes an array of logic-operation circuits and a plurality of input and output lines; and

everyone of said output lines connected to a unique set of said logic-operation circuits whereby each of said output lines connected to a different set of logic-operation circuits from every other output lines.

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